Q40

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Q60

MAINBOARD

HARDWARE DOCUMENTATION

Preliminary version 02/2001

Memory Map

Address(hex)	QL	Q40 / Q60
0000 0000 0000 BFFF	**Internal ROM 48K**	**ROM 0 96K** **(Normal: Read ROM, Write RAM** **LOWRAM: Read RAM, No Write)**
0000 C000 0000 FFFF	External ROM 16K	
0001 0000 0001 7FFF	External I/O 32K	
0001 8000 0001 BFFF	**Internal I/O 16K**	**RAM 32K**
0001 C000 0001 FFFF	External I/O 16K	
0002 0000 0002 7FFF	**Screen 0 32K**	**Screen 0 32K**
0002 8000 0003 FFFF	**RAM 96K**	**RAM up to 32608K** **(4,16,20,32MB)**
0004 0000 000B FFFF	Expansion RAM 512K	
000C 0000 000F FFFF	Peripheral ROMs 16 x 16K	
0010 0000 01FF FFFF		Up to 130432K as special option only (64,80,128MB)
FE00 0000 FE03 FFFF		**ROM 1 256K** **lower 96K are ROM 0**
FE80 0000 FE8F FFFF		**Screen 1 1024K** **32K at $FE820000 are Screen 0**
FF00 0000 FF00 0034		**Master Chip** **(Keyboard, Interrupts, Video Mode, LED, Ext. Slot Reset)**
FF00 8000 FF00 8004		**Audio-DACs**
FF01 0000 FF01 8000		**Address Decoder Chip** **(ROM Mode Selection)**
FF02 0000 FF02 1FFC		**Nonvolatile RAM 2K** **Realtime Clock**
FF40 0000 FF7F FFFF		**Extension Slot IO 1024K**
FF80 0000 FFBF FFFF		**Extension Slot MEM 1024K**

Due to incomplete address decoding, accesses to $0200 0000 .. $7FFF FFFF are mirrored to 0 .. $01FF FFFF. Accesses to $8000 0000 .. $FDFF FFFF are mirrored to $FE00 0000 .. $FFFF FFFF.

DRAM

With 16 MB installed, addresses beyond the end of DRAM access no physical device.
If 4 MB (20 MB) DRAM are installed, acesses beyond $003F FFFF ($013F FFFF) are mirrored to the (upper) 4 MB. DRAM Size Detection must recognize this. Continous DRAM tests must end at 32 MB.

Special option for up to 128 MB of DRAM

This option is not available by default. It requires a special hardware upgrade and special operating system support. If special operating system support is not available, more than 32 MB can still be installed on the mainboard, but the operating system will use only 32 MB (with 80 or 128 MB installed) or 16 MB (with 64 MB installed)

Above 32 MB, memory is non-continuos. It must be accessed as multiple chunks. Between each chunk there is a gap that must not be accessed. (Due to incomple address decoding, accessing a memory gap would be mirrored to other hardware devices and could cause a software crash.) A detailed description of memory chunks follows:

128 MB of DRAM installed:

$00028000 - $01FFFFFF (1st 32 MB)
$02028000 - $03FFFFFF (2nd 32 MB)
$04028000 - $05FFFFFF (3rd 32 MB)
$06028000 - $07FFFFFF (4th 32 MB)

80 MB of DRAM installed:

$00028000 - $01FFFFFF (32 MB)
$02028000 - $02FFFFFF (1st 16 MB)
$04028000 - $04FFFFFF (2nd 16 MB)
$06028000 - $06FFFFFF (3rd 16 MB)

64 MB of DRAM installed:

$00028000 - $00FFFFFF (1st 16 MB)
$02028000 - $02FFFFFF (2nd 16 MB)
$04028000 - $04FFFFFF (3rd 16 MB)
$06028000 - $06FFFFFF (4th 16 MB)

ROM

The complete ROM is located at $FE00 0000. The lower 96 KB of the ROM can also be read at 0 .. $0001 7FFF.

The ROM can be divided into two 128 KB parts, and a jumper or switch selects which part is accessed. (This allows to access two different operating system versions directly from ROM, if they are smaller than 128 kB each.)

ROM emulation

The ROM area 0 .. $0001 7FFF can be operated in two modes:

- Normal Mode: CPU read accesses read the data from the hardware ROM, but CPU write accesses store their data in a RAM device, which appears in the same address space. As long as the system is in Normal ROM mode, the contents of the data written into the ROM area is not visible.

- LOWRAM Mode: Read accesses go to a RAM device, write accesses are ignored, actually write-protecting the RAM device in this area, so it appears to the machine as a ROM.

(This allows ROM emulation. First you can write your own ROM image, while the original ROM is still running. Next you can switch into LOWRAM mode, which will immediately replace the original ROM by your own, previously written ROM image. Usually you would then call the reset vektor to reboot your system.)

A byte-wide write access to the address decoder chip at $FF01 0000 selects the normal mode, which is also power-up default. A byte-wide write access to $FF01 8000 selects the LOWRAM mode.

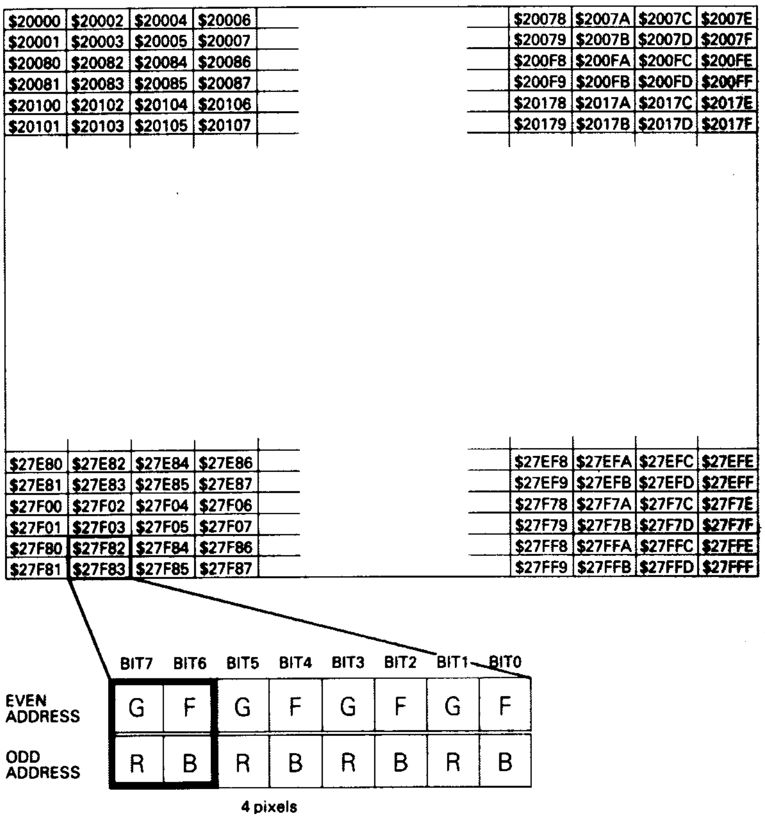
Screen

The different screen modes are set by the Display Control Register as described in chapter „Master Chip“. The complete screen area is located at $FE80 0000.

The 32 KB area beginning at $FE82 0000 can also be accessed at $0002 0000 and is used for QL modes 8 and 4.

QL Mode 8

256x256 pixel, 8 colors, 4 bits per pixel (R=Red, G=Green, B=Blue, F=Flash)
The QL mode 8 does not use the flash bit for video output, but it is present for compatibility reasons.

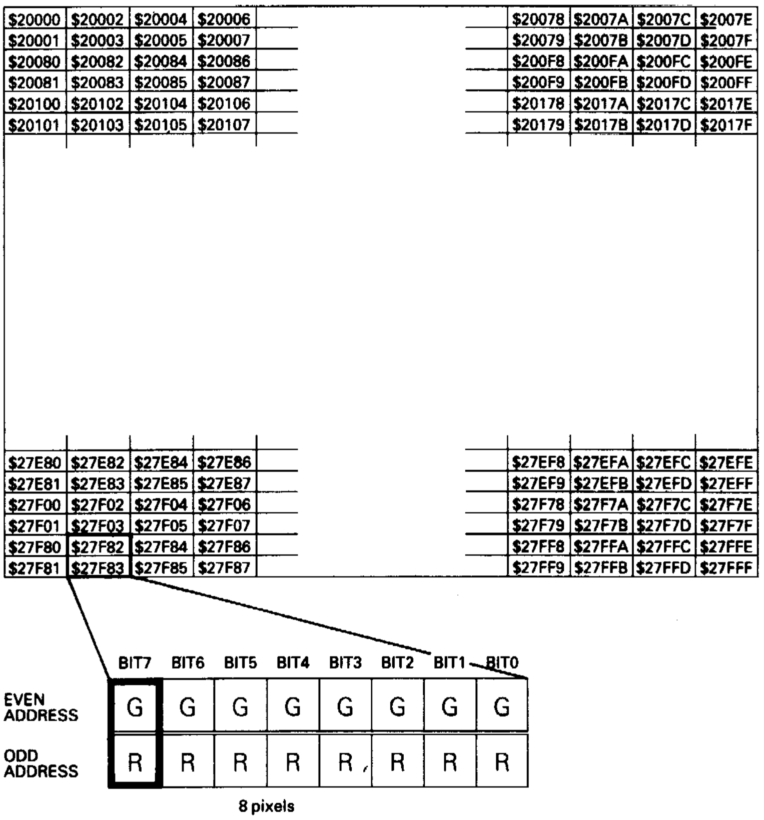


$20000	$20002	$20004	$20006		$20078	$2007A	$2007C	$2007E
$20001	$20003	$20005	$20007		$20079	$2007B	$2007D	$2007F
$20080	$20082	$20084	$20086		$200F8	$200FA	$200FC	$200FE
$20081	$20083	$20085	$20087		$200F9	$200FB	$200FD	$200FF
$20100	$20102	$20104	$20106		$20178	$2017A	$2017C	$2017E
$20101	$20103	$20105	$20107		$20179	$2017B	$2017D	$2017F
$27E80	$27E82	$27E84	$27E86		$27EF8	$27EFA	$27EFC	$27EFE
$27E81	$27E83	$27E85	$27E87		$27EF9	$27EFB	$27EFD	$27EFF
$27F00	$27F02	$27F04	$27F06		$27F78	$27F7A	$27F7C	$27F7E
$27F01	$27F03	$27F05	$27F07		$27F79	$27F7B	$27F7D	$27F7F
$27F80	$27F82	$27F84	$27F86		$27FF8	$27FFA	$27FFC	$27FFE
$27F81	$27F83	$27F85	$27F87		$27FF9	$27FFB	$27FFD	$27FFF

	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
EVEN ADDRESS	G	F	G	F	G	F	G	F
ODD ADDRESS	R	B	R	B	R	B	R	B

QL Mode 4

512x256 pixel, 4 colors, 2 bits per pixel (R=Red, G=Green)



$20000	$20002	$20004	$20006	$20078	$2007A	$2007C	$2007E
$20001	$20003	$20005	$20007	$20079	$2007B	$2007D	$2007F
$20080	$20082	$20084	$20086	$200F8	$200FA	$200FC	$200FE
$20081	$20083	$20085	$20087	$200F9	$200FB	$200FD	$200FF
$20100	$20102	$20104	$20106	$20178	$2017A	$2017C	$2017E
$20101	$20103	$20105	$20107	$20179	$2017B	$2017D	$2017F
$27E80	$27E82	$27E84	$27E86	$27EF8	$27EFA	$27EFC	$27EFE
$27E81	$27E83	$27E85	$27E87	$27EF9	$27EFB	$27EFD	$27EFF
$27F00	$27F02	$27F04	$27F06	$27F78	$27F7A	$27F7C	$27F7E
$27F01	$27F03	$27F05	$27F07	$27F79	$27F7B	$27F7D	$27F7F
$27F80	$27F82	$27F84	$27F86	$27FF8	$27FFA	$27FFC	$27FFE
$27F81	$27F83	$27F85	$27F87	$27FF9	$27FFB	$27FFD	$27FFF

	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
EVEN ADDRESS	G	G	G	G	G	G	G	G
ODD ADDRESS	R	R	R	R	R	R	R	R

High color mode 512x256 pixels, 64K colors

512x256 pixel, 65536 colors, 16 bits per pixel

G5..G1=Green, R5..R1=Red, B5..B1=Blue
RGB0: Common least significant bit for all three colors

Both high-color mode screens begins at $FE80 0000 with the upper left pixel and go left to right, up to down. Each pixel is represented by a word (two bytes), with the following bitmap:

G5	G4	G3	G2	G1	R5	R4	R3	R2	R1	B5	B4	B3	B2	B1	RGB0

The bits G5 to G1 stand for the green, R5 to R1 for the red, and B5 to B1 for the blue portion. The lowest bit RGB0 is a common least significant bit for Red, Green and Blue. The brightness of the green portion is given by:

G5*(2^5) + G4*(2^4) + G3*(2^3) + G2*(2^2) + G1*(2^1) + RGB0*(2^0)

The brightness of the red portion is given by:

R5*(2^5) + R4*(2^4) + R3*(2^3) + R2*(2^2) + R1*(2^1) + RGB0*(2^0)

The brightness of the blue portion is given by:

B5*(2^5) + B4*(2^4) + B3*(2^3) + B2*(2^2) + B1*(2^1) + RGB0*(2^0)

With the color sceme of the Q40 / Q60 it is possible to display 64 different grey levels without color error. (When displaying grey levels, you have G5=R5=B5, G4=R4=B4, ..., G1=R1=B1. Together with the common bit RGB0 there are 6 grey bits available, which give 2^6 levels.)

High color mode 1024x512 pixel, 64K colors

1024x512 pixel, 65536 colors, 16 bits per pixel

This high-color mode screen also begins at $FE80 0000 and follows the same conventions as the high color mode with 512x256 pixels.

Audio DACs

Writing to $FF00 8000 / $FF00 8004 accesses the left / right channel Digital-Analog-Converter (DAC). Each channel is 8 bit wide. The lowest analog output voltage is represented by 0, the highest by $FF.

Realtime Clock

The 8 registers of the Realtime Clock are at $FF02 1FE0, $FF02 1FE4, ... $FF02 1FFC.

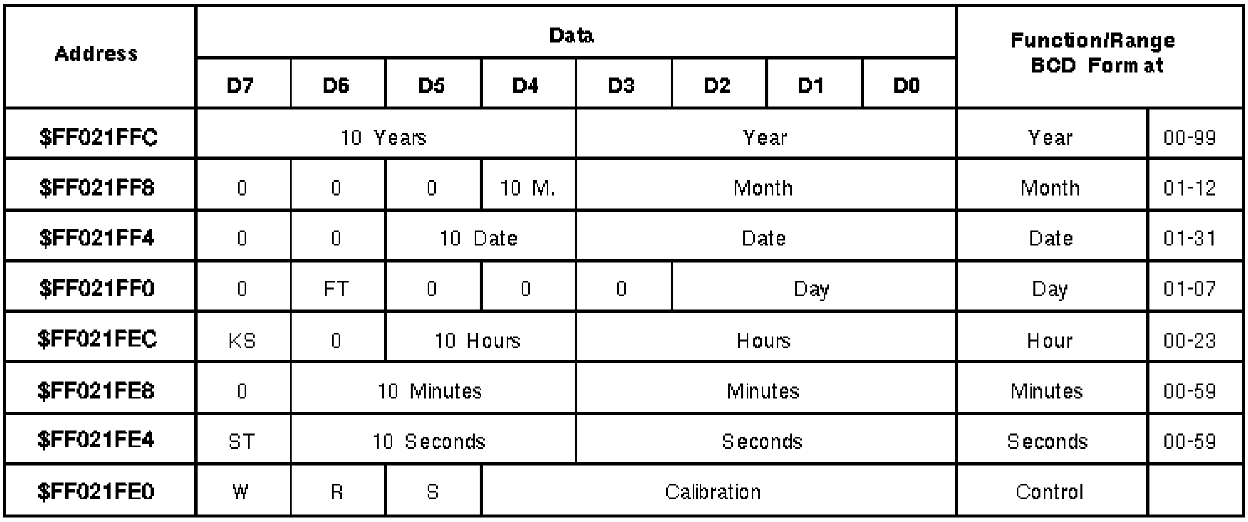
Reading the Clock

Updates to the timekeeper registers should be halted before clock data is read to prevent reading data in transition. Because the timekeeper cells in the RAM array are only data registers, and not the actual clock counters, updating the registers can be halted without disturbing the clock itself.
Updating is halted when a '1' is written to the READ bit, the seventh bit in the control register. As long as a '1' remains in that position, updating is halted. After a halt is issued, the registers reflect the count; that is, the day, date, and the time that were current at the moment the halt command was issued.
All of the timekeeper registers are updated simultaneously. A halt will not interrupt an update in progress. Updating is within a second after the bit is reset to a '0'.

Setting the Clock

The eighth bit of the control register is the WRITE bit. Setting the WRITE bit to a '1', like the READ bit, halts updates to the timekeeper registers. The user can then load them with the correct day, date, and time data in 24 hour BCD format (see Table). Resetting the WRITE bit to a '0' then transfers
the values of all time registers ($FF021FE4 .. $FF021FFC) to the actual timekeeper counters and allows normal operation to resume. The FT bit and the bits marked as '0' in the table must be written to '0' to allow for normal timekeeper and RAM operation.

Table: Timekeeper Registers



Address	Data								Function/Range BCD Format	
	D7	D6	D5	D4	D3	D2	D1	D0		
$FF021FFC	10 Years				Year				Year	00-99
$FF021FF8	0	0	0	10 M.	Month				Month	01-12
$FF021FF4	0	0	10 Date		Date				Date	01-31
$FF021FF0	0	FT	0	0	0	Day			Day	01-07
$FF021FEC	KS	0	10 Hours		Hours				Hour	00-23
$FF021FE8	0	10 Minutes			Minutes				Minutes	00-59
$FF021FE4	ST	10 Seconds			Seconds				Seconds	00-59
$FF021FE0	W	R	S	Calibration					Control	

Keys: S = SIGN Bit
FT = FREQUENCY TEST Bit (Set to '0' for normal clock operation)
KS = KICK START Bit
R = READ Bit
W = WRITE Bit
ST = STOP Bit
0 = Must be set to '0'

Stopping and Starting the Oscillator

The oscillator may be stopped at any time. If the device is going to spend a significant amount of time on the shelf, the oscillator can be turned off to minimize current drain on the battery. The STOP bit is the MSB of the seconds register. Setting it to a '1' stops the oscillator. The clock is shipped from the manufacturer with the STOP bit set to a '1'. When reset to a '0', the oscillator starts within 1 second.

Calibrating the Clock

A typical Q40 / Q60 realtime clock is accurate within +/-1 minute per month at 25° C without calibration. The realtime clock can employ periodic counter correction. The calibration circuit adds or subtracts counts from the oscillator divider circuit. The number of times pulses are subtracted (negative calibration) or added (positive calibration) depends upon the value loaded into the five bit Calibration byte found in the Control Register. Adding counts speeds the clock up, subtracting counts slows the clock down.

The Calibration byte occupies the five lower order bits in the Control register. This byte can be set to represent any value between 0 and 31 in binary form. The sixth bit is a sign bit; '1' indicates positive calibration, '0' indicates negative calibration. Each calibration step has the effect of adding 512 or subtracting 256 oscillator cycles for every 125,829,120 actual oscillator cycles, that is +4.068 or -2.034 PPM of adjustment per calibration step in the calibration register. Each of the 31 increments in the Calibration byte would represent +10.7 or - 5.35 seconds per month which corresponds to a total range of +5.5 or -2.75 minutes per month.

NOTE: The Q40 / Q60 may also come with a factory calibrated clock. In this case clock calibration has no effect.

Nonvolatile RAM

The 2040 Bytes of Nonvolatile RAM can be accessed at $FF02 0000, $FF02 0004, ... $FF02 1FDC (every 4th byte).

With valid supply voltage applied, the nonvolatile RAM operates as a conventional bytewide static RAM. Should the supply voltage decay, the RAM will automatically power-fail deselect, write protecting itself. All outputs become high impedance, and all inputs are treated as "don't care."

Note: A power failure during a write cycle may corrupt data at the currently addressed location, but does not jeopardize the rest of the RAM's content.

The power switching circuit connects external VCC to the RAM and disconnects the battery when VCC rises. As VCC rises, the battery voltage is checked. If the voltage is too low, an internal Battery Not OK (BOKn) flag will be set. The BOKn flag can be checked after power up:

1. Read Data at any address
2. Write Data complement back to same address
3. Read data at same address again
4. If data is not the complement of the first read: LOW BATTERY
5. Write original data back to same address

If the BOKn flag is set, the first write attempted will be blocked. The flag is automatically cleared after the first write, and normal RAM operation resumes.

Extension Slot

Two areas of 1024 K bytewide or wordwide accessible peripheral space.
8 bit IO: CPU Address = $FF40 0001 + 4 * Slot Address
16 bit IO: CPU Address = $FF40 0000 + 4 * Slot Address
8 bit MEM: CPU Address = $FF80 0001 + 4 * Slot Address
16 bit MEM: CPU Address = $FF80 0000 + 4 * Slot Address

Master Chip

Base address is $FF00 0000. All accesses should be byte-wide.

A level 2 interrupt request to the CPU is asserted, if any of the following occurs:

- Keycode received and keyboard interrupt enabled
- Serial interrupt line(s) active and serial interrupt enabled
- Frame interrupt every 20 ms (50 Hz) or every 5 ms (200 Hz) according to the selected frequency
- External interrupt line(s) active and external interrupt enabled

A level 4 or 6 interrupt request to the CPU is asserted every 50 us (100 us), if the sample interrupt is enabled. Sample rate is 20 kHz (10 kHz).

Interrupt Register, Offset $00

Read

Bit 0	always 0 (QL:gap interrupt)
Bit 1	1=Keycode received (QL:interface interrupt)
Bit 2	1=Serial interrupt line(s) active, from external interrupt lines 0 or 1, corresponding to ISA IRQ 3 or 4 (QL:transmit interrupt)
Bit 3	1=Frame interrupt every 20 ms (50 Hz)
Bit 4	1=External interrupt line active, from external interrupt lines 2..7 = IRQ 5,6,7,10/11,14,15

External Interrupt Register, Offset $04

Read

Bit 0	1=ext. interrupt line 0 active	IRQ 3	Com 2/4
Bit 1	1=ext. interrupt line 1 active	IRQ 4	Com 1/3
Bit 2	1=ext. interrupt line 2 active	IRQ 5	
Bit 3	1=ext. interrupt line 3 active	IRQ 6	Floppy
Bit 4	1=ext. interrupt line 4 active	IRQ 7	LPT 1
Bit 5	1=ext. interrupt line 5 active	IRQ 10/11	
Bit 6	1=ext. interrupt line 6 active	IRQ 14	IDE drives
Bit 7	1=ext. interrupt line 7 active	IRQ 15	Secondary IDE drives

Keyboard Interrupt Enable, Offset $08

Write

Bit 0	0=disable interrupt request from keyboard, the keycode received bit in the interrupt register still works (default) 1=enable interrupt request from keyboard

Offset $0C

Reserved. Do not use.

External Interrupt Enable, Offset $10

Write

Bit 0	0=disable interrupt request from external interrupt lines 2..7; the corresponding bits in the external interrupt register still work (default) 1=enable interrupt request from external interrupt lines 2..7

Sample Interrupt Enable, Offset $14

Write

Bit 0	0=disable sample interrupt request (default) 1=enable interrupt request (Level 4 or 6) every 50 us (20 kHz)

Display Control Register, Offset $18

Read/Write

Bits 1,0	0=QL Mode 8, 256 x 256 pixel, 8 colors 1=QL Mode 4, 512 x 256 pixel, 4 colors 2=High Color Mode, 512 x 256 pixel, 64K colors 3=High Color Mode, 1024 x 512 pixel, 64K colors

Keycode Register, Offset $1C

Read

Bit 7..0	Keycode, valid if the keycode received bit in the interrupt register is set

Keyboard Unlock, Offset $20

Write

*	Keyboard unlock, clear the keycode received bit in the interrupt register, remove interrupt request from keyboard

Frame Interrupt Clear, Offset $24

Write

*	Clear the frame interrupt bit in the interrupt register, remove frame interrupt request

Sample Interrupt Clear, Offset $28

Write

*	Clear the sample interrupt request (Level 4 or 6)

Sample Rate, Offset $2C

Write

Bit 0	0= Sample interrupt request (Level 4 or 6) every 100 us (10 kHz) 1= Sample interrupt request (Level 4 or 6) every 50 us (20 kHz)

LED Register, Offset $30

Write

Bit 0	0=LED off (high voltage level) (default) 1=LED on (low voltage level)

Extension Bus Reset, Offset $34

Write

Bit 0	0= Deactivate Extension Bus hardware reset 1= Activate hardware reset of Extension Bus(default) Also resets the XT Keyboard, if available

Frame Rate, Offset $38

Write

Bit 0	0= Frame interrupt request (Level 2) every 20 us (50 Hz) (default) 1= Frame interrupt request (Level 2) every 5 us (200 Hz)

Utility ROM

To support low-level development of new operating systems, and hardware tests, a utility ROM for the Q40 and Q60 has been developed. It doesn't need an operating system to run. Among other things it can download an operating system via the serial port and start it.

Download of up to 96 KB pseudo ROM code via the serial port SER1. File format:

Bytes 0...3	Lenght L of pseudo ROM code (Longword)
Bytes 4...L+3	Binary pseudo ROM code

If you can run QDOS Classic, SMSQ/E or Linux on your machine, you won't need the Utility ROM.

IDE harddisks and other IDE devices

IDE harddisks used with the Q40 or Q60 should support PIO mode 2 or faster.
(Q60 only: Incompatibilties between the Q60 and few IDE CDROM and CDRW drives have been detected.)

All specifications are subject to change without notice. No responsibility is assumed for inaccuracies or errors.